AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An identification device:

a non-resonant receiving means for receiving a first signal and employing the first signal to generate a voltage;

wherein the non-resonant receiving means generates a first current from the voltage;

an integrated circuit;

wherein the integrated circuit includes a state selection means for randomly or pseudo-randomly selecting whether the device is in a first state or a second state;

a connection between the non-resonant receiving means and the integrated circuit;

a transmission means for generating a second signal;

wherein relative to the second state, a relatively larger amount of a first current flows through the non-resonant receiving means when the device is in the first state;

wherein relative to the first state, a relatively smaller amount of the first current flows through the non-resonant receiving means when the device is in the second state; and

wherein the relatively smaller amount of the first current causes the non-resonant receiving means to not interfere with operation of a second identification device in close proximity to the identification device.

2. (Previously Presented) The identification device according to claim 1 wherein:

a first probability is associated with the first state;

a second probability is associated with the second state; and

the first probability is lower than the second probability.

3. (Previously Presented) The identification device according to claim 2 wherein the first probability is at least two times lower than the second probability.

4. (Previously Presented) The identification device according to claim 2 wherein the first probability is at least four times lower than the second probability.

5. (Previously Presented) The identification device according to claim 2 wherein the first probability is at least eight times lower than the second probability.

6. (Previously Presented) The identification device according to claim 2 wherein the first probability is at least sixteen times lower than the second probability.

7. (Previously Presented) The identification device according to claim 2 wherein the relatively smaller amount of current is at least less than approximately 100 μA.

8. (Previously Presented) The identification device according to claim 7 wherein the relatively smaller amount of current is less than approximately 50 μA.

9. (Previously Presented) The identification device according to claim 8 wherein the relatively smaller amount of current is less than approximately 30 μA.

10. (Previously Presented) The identification device according to claim 9 wherein the relatively smaller amount of current is less than approximately 15 μA.

11. (Previously Presented) The identification device according to claim 10 wherein the relatively smaller amount of current is less than approximately 5 μA.

12. (Previously Presented) The identification device according to claim 11 wherein the relatively smaller amount of current is between approximately 0.1 μA and approximately 4.99 μA.

13. (Previously Presented) The identification device according to claim 2 wherein the relatively smaller amount of the first current is less than 50% of the relatively larger amount of the first current.

14. (Previously Presented) The identification device according to claim 13 wherein the relatively smaller amount of the first current is less than 25% of the relatively larger amount of the first current.

15. (Previously Presented) The identification device according to claim 14 wherein the relatively smaller amount of the first current is less than 5% of the relatively larger amount of the first current.

16. (Previously Presented) The identification device according to claim 15 wherein the relatively smaller amount of the first current is less than 1% of the relatively larger amount of the first current.

17. (Previously Presented) The identification device according to claim 2 wherein the first probability and second probability are at least partially random.

18. (Previously Presented) The identification device according to claim 2 wherein:

the integrated circuit has an operating cycle of a first time;

the device is in either the first state or the second state and not both states during the first time; and

the integrated circuit receives the first signal for a second time.

19. (Canceled)

20. (Currently Amended) The identification device according to claim 2 wherein the non-resonant receiving means is an antenna.

21. (Previously Presented) The identification device according to claim 20 wherein the antenna is a coil.

22. (Currently Amended) The identification device according to claim 20 wherein the non-resonant receiving means is a dipole antenna.

23. (Currently Amended) The identification device according to claim 20 wherein the non-resonant receiving means is a capacitive antenna.

24. (Previously Presented) The identification device according to claim 2 wherein the first signal is at least one of: an electric signal, a capacitive signal, an inductive signal, a radio signal, and a magnetic signal.

25. (Previously Presented) The identification device according to claim 2 wherein the connection includes a voltage multiplier.

26. (Previously Presented) The identification device according to claim 2 wherein the connection includes a voltage rectifier.

27. (Previously Presented) The identification device according to claim 2 wherein the transmission means is connected to, and responsive to, a series regulator.

28. (Currently Amended) The identification device according to claim 2 wherein the device further includes a first device portion that is comprised of an impedance means in series with the non-resonant receiving means.

29. (Previously Presented) The identification device according to claim 28 wherein the impedance means is at least one of: an extra resistor, a capacitor, and an inductor.

30. (Previously Presented) The identification device according to claim 28 wherein the impedance means is a switched impedance.

31. (Previously Presented) The identification device according to claim 2 wherein the device further includes a second device portion that is comprised of the impedance means in series with the integrated circuit.

32. (Previously Presented) The identification device according to claim 31 wherein the impedance means is a switched impedance.

33. (Previously Presented) The identification device according to claim 2 wherein the state selection means is responsive to the first signal.

34. (Previously Presented) The identification device according to claim 33 wherein the first signal includes at least one or more first signal breaks, and the state selection means is responsive to the first signal breaks.

35. (Previously Presented) The identification device according to claim 2 wherein the device further includes a memory.

36. (Previously Presented) The identification device according to claim 35 wherein the memory includes memory space for at least one of the following information units: content information, address information, and name information.

37. (Previously Presented) The identification device according to claim 2 wherein the device has a thickness between 0.0 mm and 0.5 mm.

38. (Previously Presented) The identification device according to claim 2 wherein the device has a width between 10 mm and 10 cm, and a length between 60 mm and 100 mm.

39. (Previously Presented) The identification device according to claim 2 wherein the integrated circuit includes an onboard power source.

40. (Previously Presented) The identification device according to claim 2 wherein the device employs a second antenna means, that is responsive to the integrated circuit, to generate the second signal.

41. (Currently Amended) The identification device according to claim 2 wherein the non-resonant receiving means is also the transmission means.

42. (Previously Presented) The identification device according to claim 41 wherein the transmission means is responsive to the integrated circuit for generating the second signal.

43. (Previously Presented) The identification device according to claim 2 wherein the state selection means includes a MOSFET transistor.

44. (Currently Amended) A system for identifying articles comprising:

a signal generator for generating a first signal;

a plurality of identification devices, each individual device being respectively associated with each individual article;

wherein each device comprises:

a non-resonant receiving means for receiving the first signal and employing the first signal to generate a voltage;

wherein the non-resonant receiving means generates a first current from the voltage;

an integrated circuit;

wherein the integrated circuit includes a state selection means for randomly or pseudo-randomly selecting whether the device is in a first state or a second state;

a connection between the non-resonant receiving means and the integrated circuit;

a transmission means for generating a second signal;

wherein relative to the second state, a relatively larger amount of the first current flows through the non-resonant receiving means when the device is in the first state;

wherein relative to the first state, a relatively smaller amount of the first current flows through the non-resonant receiving means when the device is in the second state; and

wherein the relatively smaller amount of the first current causes the non-resonant receiving means to not interfere with operation of a second identification device in close proximity to the identification device.

45. (Previously Presented) The system according to claim 44 wherein each device further includes a memory.

46. (Previously Presented) The system according to claim 45 wherein the memory includes memory space for at least one of the following information units: content information, address information, and name information.

47. (Previously Presented) The system according to claim 46 further including a sorting means that sorts the articles according to at least one of the following information units: content information, address information, and name information.

48. (Currently Amended) The system according to claim 47 wherein the plurality of devices are placed as close as 0 cm of each other without interfering with their respective non-resonant receiving means' ability to receive the first signal and their respective transmissions means' ability to generate the second signal.

49. (Previously Presented) The system according to claim 47 wherein the articles are documents.

50. (Previously Presented) The system according to claim 47 wherein the articles are parcels.

51. (Previously Presented) The system according to claim 47 wherein the articles are postaged articles including at least: letters, and packages.

52. (Previously Presented) The system according to claim 47 wherein the articles are baggage.

53. (Previously Presented) The system according to claim 47 wherein the articles are inventory-related items.

54. (Previously Presented) The system according to claim 44 wherein:

a first probability is associated with the first state;

a second probability is associated with the second state; and

the first probability is lower than the second probability.

55. (Previously Presented) The system according to claim 44 wherein the first probability is at least two times lower than the second probability.

56. (Previously Presented) The system according to claim 44 wherein the first probability is at least sixteen times lower than the second probability.

57. (Previously Presented) The identification device according to claim 2 wherein the state selection means is comprised of a plurality of digital circuits.

58. (Previously Presented) The identification device according to claim 57 wherein the digital circuits are comprised of one of the following: a dedicated logic circuit consisting of logic gates, a state engine consisting of logic arrays, a micro controller, and a processor.

59. (Previously Presented) The identification device according to claim 57 wherein the digital circuits are comprised of a plurality of logic arrays.

60. (Previously Presented) The identification device according to claim 59 wherein the logic arrays are controlled by a microcontroller.

61. (Currently Amended) A method for interrogating an identification device comprising the steps of:

providing an identification device having an integrated circuit, a non-resonant receiving means connected to the integrated circuit and a transmitting means;

receiving a first signal within the non-resonant receiving means and employing the first signal to generate a voltage;

generating a first current from the voltage;

randomly or pseudo-randomly selecting a first or second state for the identification device, wherein a relatively larger amount of the first current flows through the non-resonant receiving means when the device is in the first state and wherein a relatively smaller amount of the first current flows through the non-resonant receiving means when the device is in the second state; and

wherein the relatively smaller amount of the first current causes the non-resonant receiving means to not interfere with operation of a second identification device in close proximity to the identification device.

62. (Previously Presented) The method of claim 61, wherein:

a first probability is associated with the first state;

a second probability is associated with the second state; and

the first probability is lower than the second probability.

63. (Previously Presented) The method of claim 61, wherein:

the integrated circuit operates in an operating cycle having a first time;

the identification device operates in either the first state or the second state and not both states during the first time; and

the identification device receives the first signal for a second time.

64. (New) The identification device according to claim 21 wherein the coil does not include a resonating capacitor.

65. (New) The identification device according to claim 21 wherein a resonating capacitor is not connected to the coil.

66. (New) The identification device according to claim 21 wherein the coil is not tuned by a tuning capacitor.